Common Fallacies about Multivalued Circuits

Daniel Etiemble
Computer Science Laboratory (LISN)
Paris Saclay University
Orsay, France

***Abstract*—For more than 60 years, many ternary or quaternary circuits have been proposed based on similar assumptions. We successively examine four of these assumptions and demonstrate that they are wrong. The fundamental reason for which m-valued combinational circuits are more complicated than the corresponding binary ones is explained. M-valued flash memories are used in USB devices because access times in not critical and a trade-off is possible between access time and chip area. If m-valued circuits are reduced to a very small niche in the binary world with semi-conductor technologies, there is a significant exception: quantum devices and computers are a true breakthrough as qbits are intrinsically multivalued. Successful m-valued circuits need m-valued devices as qbits.**

I. Introduction

In 1958, a ternary computer called Setun has been developed at Moscow State University [1]. It was probably the first significant m-valued computer. From the late 50', many multivalued circuits have been proposed using different circuit technologies.

Different arguments have been used to justify these proposals:

- For computation, radix R = 3 would be more economical than R = 2 because the "optimal" radix would be R = e = 2.718, according to a demonstration presented in [2]. The same argument can be found in many proposals of ternary circuits. A typical quote is: "The most efficient multiple-valued system, which leads to the least product cost and complexity, is ternary logic" [3].
- Multivalued circuits having more logical states, more information could be transmitted through wires, reducing the amount of interconnections inside and outside a chip. This second argument can be found in nearly every proposal of m-valued circuits. We just present one among a lot of similar quotes: "One of the main problems in binary logic is the high volume of interconnections which can increase the chip area and power consumption" [4].
- "The modern CMOS technologies face significant complications in nanotechnology circuits such as tight channel effect and high current leakages" [5] and "Among all different transistor technologies, CNTFET has a higher performance" [6]. As m-valued circuits are easier to design with CNTFET technology, this technology could open space for m-valued circuits.
- A new argument is becoming popular. As the commonly used modern CMOS technologies are closed to an end with the 1-nm node, the post-CMOS era is supposed to be a beyond-binary era. This is the argument used in [7].

We are faced to a significant contradiction. M-valued circuits are supposed to be better than the binary ones. At the same time, the predominance of binary circuits has never been so evident. So, either the IC designers of binary circuits don't know the advantages of m-valued circuits, or the supposed advantages of m-valued circuits are based on wrong assumptions.

In this paper, we examine the following assumptions and show that they are wrong:

- Is 3 the best radix for computation?
- M-valued interconnects
- CNTFET technology to overcome the limitations of modern CMOS technologies
- M-valued circuits with emerging technologies
- End of Moore's law and post-CMOS technologies

We finally detail why the m-valued circuits are restricted to a small niche in the binary world, with only one significant exception: quantum computing as qbits are intrinsically m-valued devices.

II. Is 3 the best radix for computation?

This assumption has been formulated in a paper [2] that is quoted by most designers of ternary circuits. As the optimal radix would be e=2.7, R=3 is the best radix for computation.

A. The Hurst demonstration

The number of digits necessary to express a range of N is given by N=R^d, where R is the radix and d the number of digits, rounded to the next highest value. It is assumed that the complexity C of the system hardware is proportional to the digit capacity $R \times d$ where k is a constant.

$$C = k(R \times d) = k(R \times \frac{logN}{logR}) \quad (1)$$

Differentiating with respect to R shows that R = e for a minimum cost C.

Fig. 1 shows that the curve complexity = f(R) for radixes 2 to 16 presents a minimum close to R = 3. Figure 2 is a zoom of Figure 1 for R = 2 to 4.

Fig. 2 leads to two different remarks:

- There is a minimum value for R = e, but the curve is very flat. $C(e) = 2.718$ while $C(2) = 2.885$ and $C(4) =$

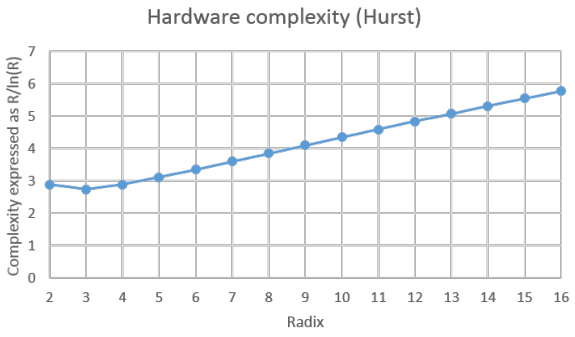

Fig. 1. Hardware complexity for Radixes 2 to 16

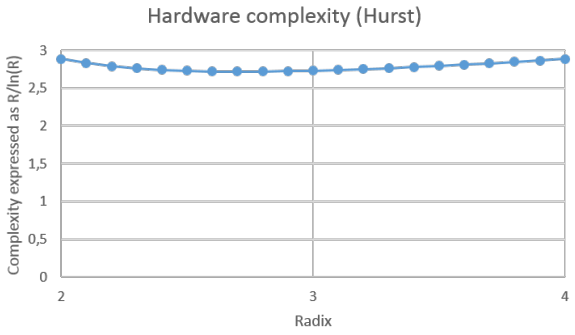

Fig. 2. Hardware complexity for Radixes 2 to 4

2.885. The difference between C(2) and C(3) is 5.66%. Is such a difference sufficient to claim that ternary circuits are more efficient than binary ones?

- It turns out that C(2) = C(4). Does binary circuits and quaternary circuits carrying the same amount of information have the same hardware complexity? It is very easy to find 4-valued circuits that are far more complex than the two corresponding binary ones. Such an example is provided below.

B. Comparison of two binary inverters with one 4-valued inverter

Fig. 3 presents a 4-valued CNTFET inverter that has been presented in Microelectronics Journal in 2015 [8]. At that point in the discussion, there is no need to give details on the CNTFET technology as we compare transistor counts in the same technology. A 4-valued inverter carries 2 bits of information. Two binary inverters also carry 2 bits of information and use $2 \times 2 = 4$ transistors. The 4-valued inverter has 6 transistors plus 2 binary inverters for a total of 10 transistors. The 4-valued inverter has 10/4 = x2.5 more transistors. In Fig. 3, two binary inverters being included in the right part of the figure, transistors T1 to T6 are the overhead of the 4-valued approach over the binary one! More, the 4-valued inverter needs three voltage supplies ($V_{dd}/3$, $2V_{dd}/3$ and V_{dd}) while the binary inverter only uses one. Many other examples could be provided with different technologies and different circuit styles. This result is not surprising. The binary values 00, 01, 10 and 11 are organized according to the Boolean lattice: each binary inverter has only one threshold level. The quaternary values are totally ordered: $0 < 1 < 2 < 3$ and the 4-valued inverter has 3 threshold levels. The number of threshold levels affects the hardware complexity.

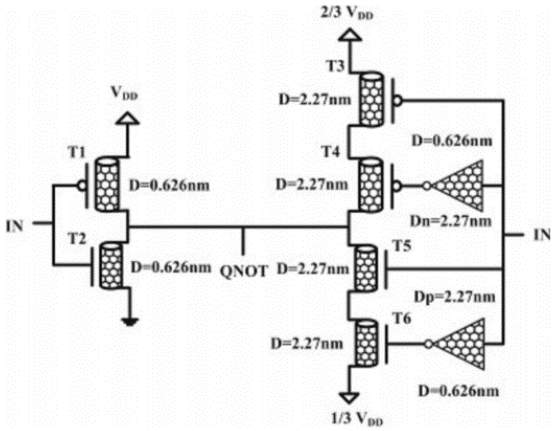

Fig. 3. A 4-valued CNTFET inverter [8]

C. Comparing quaternary and binary full adders

The presented quaternary inverter (Fig. 3) is not an exception. Table I presents the transistor count of different proposed quaternary adder with the 28 T conventional implementation of the binary full adder (there are many implementations of the binary full adder using less than 28 T).

D. 3 is not the best radix for computation

Hurst's assumption has been disproved. For people that are not yet convinced, just try to compare the number of binary devices that have been fabricated and used in the last 60 years with the number of ternary circuits!

III. M-VALUED INTERCONNECTS?

M-valued interconnects can be used in two different ways:

- All the interconnects of the circuits are m-valued.
- M-valued interconnects are used between binary building blocks.

A. Internal m-valued connects

It is obvious that an m-valued signal carries more information than a binary signal.

- A binary signal carries 1 bit.
- A ternary signal carries $log(3)/log(2) = 1.585$ bits
- A 4-valued signal carries $log(4)/log(2) = 2$ bits

TABLE I
TRANSISTOR COUNT FOR QUATERNARY AND BINARY FULL ADDERS

	[9] from [10]	[11]	2 binary adders
Transistor count	154	83	56

This property is used by most MVL designers to claim that m-valued circuits reduce the interconnection issues. But this assumption is debatable.

- It is true when considering 4-valued signals between binary circuits or when considering input and output signals of an m-valued circuit.
- But the assumption becomes false when the m-valued circuits has many more transistors that the corresponding binary ones, with many more internal m-valued connects. This point is forgotten by many MVL designers.

Published papers on m-valued circuits generally provide the electrical scheme. It delivers a limited information on the interconnections. The interconnection features can only be evaluated at the layout level, as interconnections are implemented as poly and different metal layers in CMOS (FinFET) and CNTFET technologies. For instance, Fig. 4 and Fig. 5 respectively present the layout and the circuit scheme of a 2-input multiplexer [12]. All the connections are not shown in the electrical scheme. The connections are implemented as Metal 2 (blue), Metal 1 (violet) and polysilicon (pink). M-valued circuit proposals generally present the electrical schemes, the switching performance by using electrical simulators, but they rarely or never present the layout. However, considering the connections at the transistor level gives insight on the interconnections at the layout levels. There are few possibilities that more connections at the transistor levels lead to less interconnections and less chip area at the layout level. If there are significant differences between number of connections at transistor level for m-valued and binary circuits, we can easily assume that the situation is similar at the layout level.

The 4-valued inverter presented in Figure 3 has one 4-valued input and one 4 valued output while the two corresponding binary inverters have 2 inputs and 2 outputs. However, the electrical scheme of the 4-valued inverters shows far more internal interconnects than the 2 internal interconnects of the 2 binary inverters. As already mentioned, the two binary inverters being included in the 4-valued inverter, the 4-valued inverter has many more internal connects. We could multiply the number of examples with the huge number of published papers on ternary full adders and multipliers or quaternary adders. We just provide some figures:

- The transistor count of published ternary full adders has decreased from 142 T [13] down to 56 T (not yet published paper). It seems that this value is close to the minimal value. This is to be compared to the conservative implementation of binary full adder (28 T). The transistor count ratio is 56/28 = 2, which is greater than the 1.585 information ratio between ternary and binary signals.
- The transistor count of ternary multiplier ranges from 112 T [14] down to 26 T [15] while the binary multiplier is just a AND gate (6 T).

It should be mentioned that the interconnect technologies are still improving with 3D interconnects.

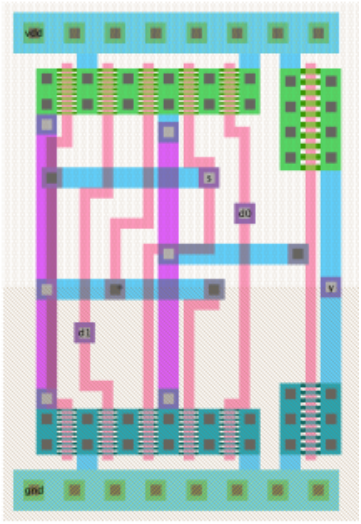

Fig. 4. 2:1 CNTFET multiplexer layout

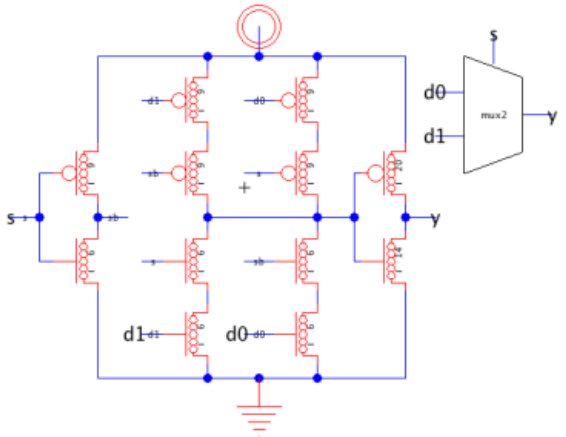

Fig. 5. 2:1 CNTFET multiplexer circuit

B. M-valued interconnects between binary circuits

1) Dividing by two the number of interconnects: In that case, it means that binary circuits are used for computation and m-valued encoder and decoder circuits are used to interconnect large blocks of binary circuits. The natural solution is then to use 4-valued signals to divide by two the number of interconnects, according to Figure 6. This idea is not new. For instance, we proposed it 40 years ago for TTL circuits [16]. However, this approach has never been used by industry. The industrial solution for interconnects has been to double the number of interconnects with high-speed serial links.

2) Doubling the number of interconnects: For "long distance" or "high-speed" transmissions, differential signals are used instead of single end signals, as shown in Fig. 7. Differential signaling has advantages over single-ended signaling to guaranty signal integrity such as:

- Better noise margins, as the signal swing is the difference between positive and negative signals

- Self-reference as the threshold is (positive signal + negative signal=/2).
- Reduced switching time due to lower voltage swing.
- Subtraction between positive and negative signals rejects common-mode noise.

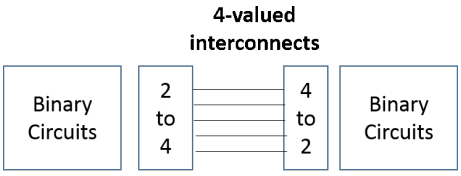

Fig. 6. 4-valued interconnects between binary circuits

While differential links are used at physical level, different buses and links have been defined and used in computer architectures. There are many examples: SuperSpeed USB 3.0 [17], PCIe [18], XAUI [19], InfiniBand [20], RapidIO [21], and SATA [22]. We give some more details only for two of them.

- PCI Express is a high-speed serial bus. A PCI express link (or interconnect) between two devices consists in a number of lanes, each lane being composed of two differential signaling pairs, one for receiving data and the other one for transmitting. Successive versions have been defined. PCI Express 1.0 has been introduced in 2003 and PCI Express 5.0 specifications have been released in 2019.
- NVLink: To improve the interconnection bandwidth between CPU and GPUs, NVidia introduced a new interconnect architecture called NVLink [23]. A single NVLink is a bidirectional interface incorporating 32 wires forming eight differential pairs in each direction. The first implementation NVLink1 was introduced in the Tesla P100 GPU (2016). Each link has a 40 GB/s bidirectional bandwidth. NVLink1 is also used by IBM in the Power8 microarchitecture. NVlink2 was introduced with GV100 GPU (2018). Bidirectional bandwidth was 50 GB/s.

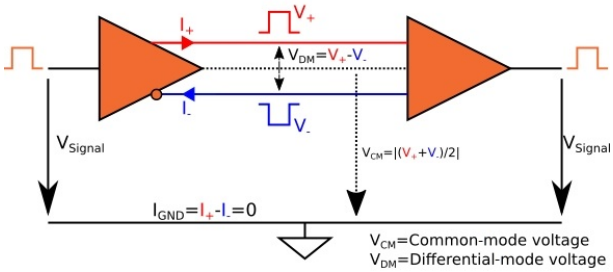

Fig. 7. Differential signaling

IV. CNTFET TECHNOLOGY TO OVERCOME THE LIMITATION OF MODERN CMOS TECHNOLOGIES WITH M-VALUED CIRCUITS?

For m-valued designers, CNTFET technology has a big advantage over CMOS: the threshold level of a CNTFET only depends of the diameter of the transistor. With CMOS technologies, the threshold level (Vth) of a transistor depends on technological parameters. As CNTFET and CMOS technologies share the same circuitry styles, CNTFET technology looks like a valuable alternative to implement m-valued circuits. Different papers have compared propagation delays and power dissipation of CMOS and CNTFET technologies with the same channel length. These comparisons are done for small circuits such as inverters or ALUs. While these papers evaluate propagation delays and power dissipation, they don't consider larger circuits that could be compared to the most recent FinFET circuits.

A. Integration density

In 2012, IBM announced a breakthrough in nanotube computer chip fabrication [24]. The circuit had 10,000 CNTFETs. The IBM researchers announced: "Carbon nanotubes have the potential in the development of high-speed and power-efficient logic applications. However, for such technologies to be viable, a high density of semiconducting nanotubes must be placed at precise locations on a substrate" and "This new placement technique is readily implemented, involving common chemicals and processes, and provides a platform for future CNTFET experimental studies". Other breakthroughs were announced in 2017 [25], but it looks like IBM now focuses more on a successful technology (quantum computing) than on CNTFET technology. In 2013, the first carbon nanotube computer has been announced [26] by a Stanford group. It was a significant advance for this technology. However, this 178 CNTFETs "one-instruction-set computer" only runs at 1 KHz. The first commercial microprocessor (Intel 4004) had 2300 transistors and run at 780 KHz in 1971. In 2019, a 16-bit RISC microprocessor has been built with 14,000 CNFET transistors [27] by the same Stanford group. While this is a significant advance for CNTFET technology, we may observe that the Intel 8086 CPU, which was a 16-bit microprocessor, has been launched in 1978 with 29,000 transistors, more than 40 years ago! In 2019, the largest transistor count in a commercially available microprocessor was 39.54 billion MOSFETs, in AMD's Zen 2 fabricated using TSMC's 7 nm FinFET semiconductor manufacturing process. In 2020, the largest transistor count in a GPU (NVidia Ampere) was 54 billion transistors with the same 7 nm process. The CNTFET 16-bit microprocessor manufacturing process had 5 metal layers, while the number of metal layers in nano-CMOS technologies ranges from 8 to 15, with a trade-off between integration and cost. So, presenting CNTFET as a solution to overcome the limitation of modern FinFET technologies is more than debatable.

B. Moore law is still there

While interconnection issues have been quoted by circuits designers as a reason for proposing m-valued circuits, it turns out that the power dissipation has been the main factor driving the evolution of CMOS technologies and circuitries, even before the "heat wall" has been coined [28]. Power supply

values have been reduced, from 12 V for the first pMOS circuits down to 5V and down to a value in the 0.8 to 1V range in every technology used since 2006 (65 nm node). Fig. 8 presents the scaling of V_{dd} since the 1000 nm node. In 2000 with 130 nm node, V_{dd} value was already as low as 1.3 V. This scaling of V_{dd} means that the voltage swing available for implemented m-valued circuits is reduced to the minimal value used by binary circuits.

Techniques have been found to reduce leakage currents such as 3D FinFETs [29] (Figure 9) that reduce the leakage current by one order of magnitude.

As a result of Moore's law, new generations of CMOS/FinFET technologies, called a technological node, are regularly launched. The different successive nodes are shown in Figure 10. 7nm nodes are used since 2018-2019, 5nm since 2020 and 4 nm and 3 nm nodes have already been announced even only few companies have the financial means to build and operate the corresponding fabs.

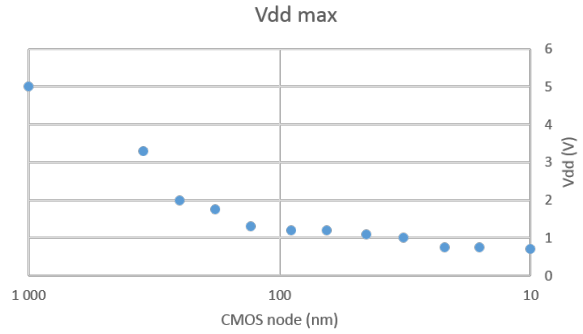

Fig. 8. V_{dd} scaling since 1000-nm node

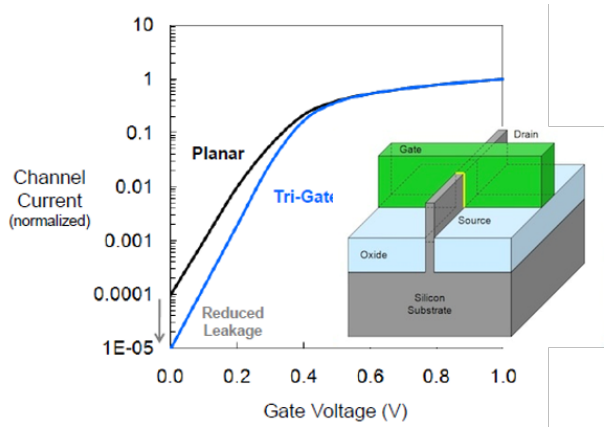

Fig. 9. Trigate transistors

If CNTFET technology can show some advantages at small scale integration level, there is no opportunity for CNTFET fabs as long as Moore's law will be there. If this opportunity occurs in the future with the end of Moore's law, it doesn't mean that the CNTFET m-valued circuits will be more efficient that the CNTFET binary circuits.

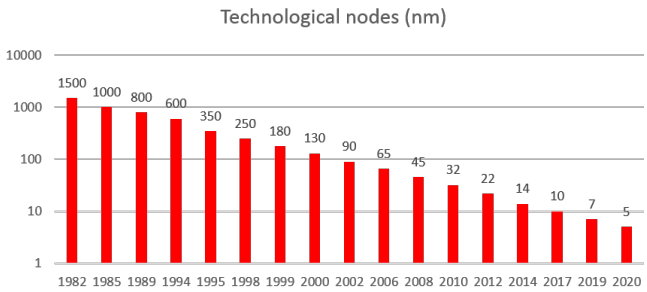

Fig. 10. CMOS technological nodes

V. M-VALUED CIRCUITS WITH EMERGING TECHNOLOGIES?

A. *Single-Electron Transistor*

Fig. 11 presents the schematics of a Single-Electron Transistor (SET). This device can be used in M-valued circuits or M-valued memories as it has several thresholds in the non-monotonic, oscillatory I_D-V_G characteristics.

A lot of papers have been presented in the 90s and far less in the last two decades. SET devices had to solve two types of problems:

- Being able to operate at normal temperature, as SET devices don't exhibit such a performance advantage to justify to operate at very low temperature like quantum devices.
- Being combined with CMOS technology to overcome the intrinsic limits of SET-only technology.

In 2012, paper [30] shows that the two issues can be solved, at least by the French CEA LETI.

The multithreshold transfer characteristics can thus be used to implement M-valued circuits. Fig. 12 shows the SET periodical literal circuit from which different M-valued gates can be derived [31]. Actual comparisons between M-valued performance and the corresponding binary ones are still to be done.

While SET technology has improved in the last decade, it is still far from being a serious competitor for classical FinFET or SOI CMOS technologies.

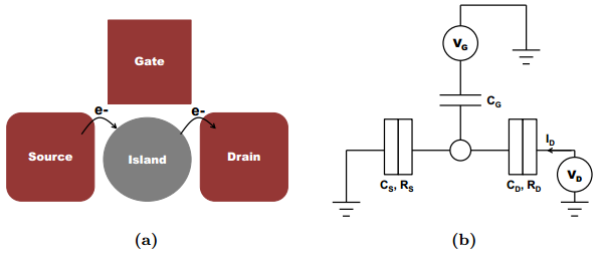

Fig. 11. (a)Schematic of SET ; (b) Schematic of equivalent circuit

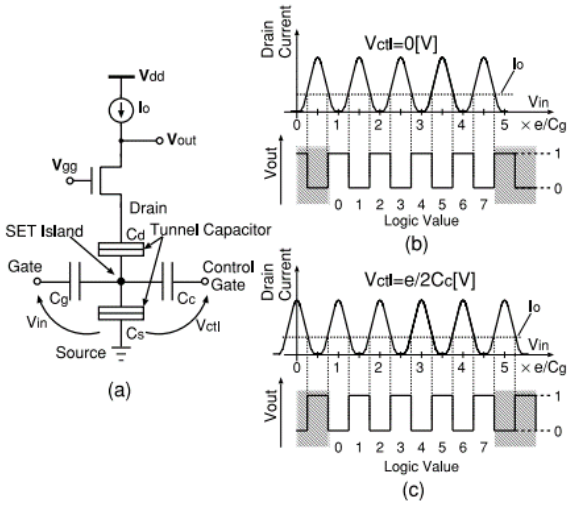

Fig. 12. SET periodical literal circuit (a)Schematic, (b) and (c) transfer characteristics for two V_{ctl} values

B. Other technologies

This paper does not pretend to consider all the technologies likely to allow the realization of m-valued circuits. For instance, a recent paper shows the potential of Resistive random access memory (ReRAM) [32] for implementing ternary logic. Again, a comparison with the corresponding binary circuits is needed.

VI. End of Moore's law, post-CMOS and post-binary

Moore's law is still there. In 2021, IBM has just announced a 50 billion transistor chip with 2 nm technology [33]. However, the launching of new nodes will not continue for ever, as physical issues are there. 1-nm node is often presented as the last one. However another debatable assumption can be noticed. The end of Moore law is often presented as the end of binary circuits . A typical example is [7] that consider multivalued technology as a solution for the "Beyond-Binary era". Are M-valued circuits better than binary circuits? Assuming a perfect performance scaling between binary and m-valued circuits, it is limited to the information ratio, i.e. 1.585 for ternary circuits and 2 for the quaternary one. It would be a "one shot" speed-up for any technology, even for a new one yet to be discovered. This situation can be compared with Moore's law that roughly provided a yearly x1.5 performance improvement! So, the post-CMOS era will probably still be binary! More, it is easy to show that the m-valued approach is less efficient than the binary one for a reason that is detailed in the next section.

VII. Totally ordered sets of values

This section doesn't deal with a misconception about m-valued circuits: it resumes the main reason why m-valued circuits are reduced to a small niche [34]. Except for the quantum technology (a q-bit is intrinsically m-valued), the

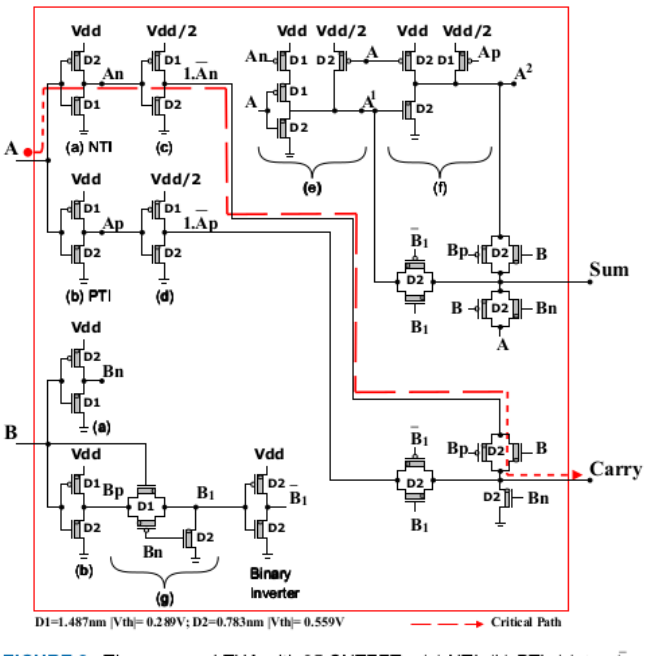

Fig. 13. A ternary Half Adder

different m values are totally ordered, either with voltage levels (combinational circuits) or with charge levels (memory circuits). This is also the case for most of the emerging new technologies. We do not consider different levels of currents as current-mode circuits imply a significant static power dissipation, which should be eliminated or reduced in modern ICs.

A. M-valued combinational circuits

We illustrate the issue with the design of a ternary half-adder for which 0 < 1 < 2. The results can be easily extended to full adders or multiplier or any ternary or quaternary combinational circuits. A good example is the ternary half adder [15] shown in Figure 13: it is probably one of the most efficient proposed ternary half adder that is based on the MUX approach. The truth table of a ternary half adder is shown in Table III. The mux approach is based on the following observation of Table III:

- When B=0 then Sum=A
- When B=1 then Sum = (A+1) mod(3) quoted as A^1
- When B=2 then Sum = (A+2) mod(3) quoted as A^2
- When B=0 then Carry=0
- When B=1 then Carry=1 when A=2 else 0
- When B=2 then Carry=1 when A>0 else 0

As the ternary values are totally ordered, specific circuits are needed to transform ternary signals into binary ones and binary signals into ternary ones.

- Decoder circuits: Binary inverters with threshold between levels 0 and 1 (called Negative inverters) and threshold between levels 1 and 2 (called Positive inverters) transform the ternary inputs in binary values. They are quoted

TABLE II
NI AND PI BINARY FUNCTIONS

	NI	PI
0	2	2
1	0	2
2	0	0

TABLE III
HALF ADDER TRUTH TABLE

	SUM				CARRY		
A/B	0	1	2		0	1	2
0	0	1	2		0	0	0
1	1	2	0		0	0	1
2	2	0	1		0	1	1

as (a) and (b) in Figure 13 and implement the truth table shown in Table II.

- Encoder circuits: They correspond to the circuits implementing the unary functions A^1 and A^2 that are quoted (e) and (f) in Figure 13. Circuits (c) and (d) are used to generate value 1 needed for the carry output.

While the typical multiplexer implementation uses transmission gates, a simplified multiplexer is used to switch A, A^1 or A^2 to the Sum output according to B value. Another simplified multiplexer switches either 0 or 1 to the carry output. This design is close to the best possible implementation of a ternary half-adder. It has only 35 CNTFETs. However, it is impossible to avoid decoding and encoding between ternary and binary values. The situation is quite different for the binary half adder for which Sum = A xor B and Carry = A and B.

Using the same MUX technique, the binary half-adder is shown in Figure 14. It uses 12 T. Permuting the MUX inputs and adding an output inverter would lead to 14 T with restored output levels. The transistor count is then the same as a typical conventional approach used in standard cell libraries [35], as shown in Figure 15 .

A ternary half adder processes x1.585 more information than the corresponding binary one. It uses 35/12 = x2.9 more transistors!

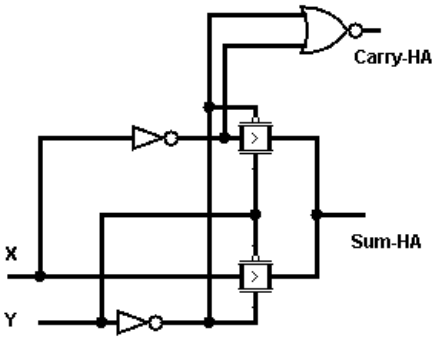

Fig. 14. Binary Half Adder (MUX technique)

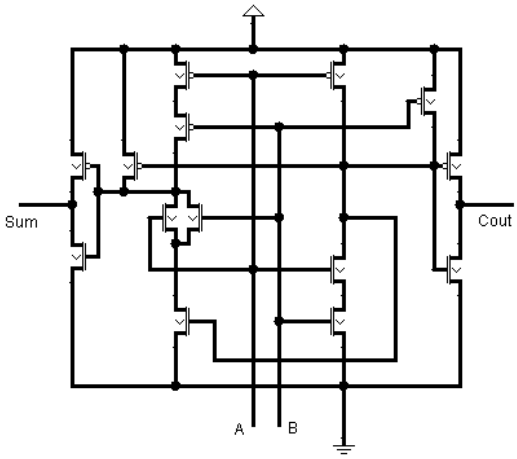

Fig. 15. 14 T binary Half Adder)

B. M-valued memory circuits

A review of multiple-valued memory technology has been published in the late 90s [36]. M-valued ROM, Flash, DRAM and CAM have been implemented and tested. It is probably the most successful area for M-valued circuits.

For M-valued ROMs, two techniques can be used:

- The first technique stores one out of four states within a single cell, keeping cell size unchanged. Each cell consists of a MOS transistor having one out of four impedance values $Z_0 < Z_1 < Z_2 < Z_3$, which correspond to different transistor channel lengths, programmed at the diffusion or polysilicon level. Reading a cell is done by comparing the cell impedance with reference transistor impedance $Z_{0.5}, Z_{1.5}$ and $Z_{2.5}$. The overall cell area is thus divided by two compared to binary ROMs, with an overhead for the comparator and decoder circuits. Details on different old commercial circuits can be found in [36]..
- The second technique also store one of four states in a single cell, but with a transistor having one of four different threshold voltages. The threshold detection of a cell is realized by linearly ramping the input of the transistor. When the input reaches the threshold level of this transistor, it turns on. This approach can be used when the access time is not the objective.

M-valued DRAM have also been presented. $2^N = M$ different possible charges are stored in the capacitance C_s of a DRAM transistor cell. In the write-mode operation, a descending 2^N-level staircase is applied is applied to the word line, i.e. to the selected transistor. For the i^{th} level input, the data line voltage is changed from low to high when the pulse level is i. In the read-mode operation, an ascendant staircase pulse is applied to the word line. The same pulse is transferred to a dummy cell, which transistor has a $C_s/_2$ capacitance for signal comparison: it is obvious that cycle time to read or write is long, as it depends on the number of levels of the staircase pulse. If density is multiplied by N, a part of the read or write cycle time is multiplied by 2^N while the other

part corresponds to the charge transfer preamplifier and the sense amplifier timing characteristics.

M-valued SRAMs and DRAMs have been fabricated and tested by industrial companies in the 80's and the 90's, such as Hitachi [37], NEC [38] and [39], etc. They are detailed in [36]. During the following decades, there was no longer such presentations by industrial companies. The main reason is that the V_{dd} level that is used by the successive nodes is too small to use the previously used techniques with conventional technologies.

M-Valued flash memories also use similar techniques and were presented in the 90s [40], [41]. They are now largely used. 4-valued (MLC) flash memories store two bits per cell. 8-valued (TLC) memories store 3 bits per cell. In 2018, ADATA, Intel, Micron, and Samsung have launched some SSD products using QLD NAND-memory with 4 bits per cell. While binary flash memories have the advantage of faster write speeds, lower power consumption and higher cell endurance, M-valued flash memories provide higher data density and lower costs

VIII. Conclusion

There are objective reasons why binary circuits are so dominant. They have replaced analog circuitry in many applications. Even if the doubling of transistors according to Moore's law is slowing down, new technological nodes are defined and used (5 nm since 2020). In the future, there will be an end for currently used and dominant technologies. However, there is no reason to predict that m-valued circuits will be a valuable alternative solution, even in they can be used in small niches such as flash memories used in USB devices.

We have examined several false assumptions concerning m-valued circuits.

- R=3 is not the best radix for computation.
- For combinational circuits, m-valued circuits have more interconnects than the binary ones when considering both external and internal connects. The transistor count ratio between m-valued circuits and the corresponding binary ones is always greater than the information ratio defined as log(m)/log(2).
- CNTFET technology has not the integration density to solve the issues of current FinFET technologies.
- The end of Moore's law does not imply the end of binary computation.

For more than 60 years, MVL researchers have unsuccessfully tried to prove the advantages of multivalued circuits. However, successful m-valued computers exist: they are called quantum computers. There is one big lesson resulting from the last 60 years. To get successful m-valued circuits, you need devices that can exhibit multiple unordered values.

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