Validation of New Substrate Design for the Improvement of Strip Warpage on LGA packages

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ABSTRACT

Land grid array or LGA package of semiconductor has been commonly used on our modern technology, from home gadgets up to industrial uses. Improvements to correct product defects and process issues are introduced to have quality products for customer satisfaction. Substrate warpage have been affecting production performance on semiconductor manufacturing. The unacceptable response results to loss of productivity losses and yield detraction. Different process improvements have been experimented to contain the problem, but results are not maintained and found to be not robust. This is where design innovation plays the part. Solder mask opening on the base material of the substrate is considered to have a favorable response after subjecting it to different environment conditions. From fast indexing and machine movement up to high thermal application on oven curing, having a robust solder mask design makes the unit acceptable and with quality. Product design as mentioned takes on another level to address the phenomenon of substrate warpage. This manuscript will be discussing how the solder mask of the substrate is optimized to achieved minimal or zero substrate warpage by performing different experiments on process and the product itself. Statistical analysis has been the basis for the implementation of the newly validated substrate design.

Keywords: Front-of-Line, Land Grid Array, MEMS, Solder Mask Opening, Substrate Design, Warpage

1. INTRODUCTION

In the fast-pacing technology and innovation all around the globe, every industry strives for limitless and continuous improvement. Companies with manufacturing plants, services and labor demands on the open market are seizing all opportunities for a better product that customers expect on them. Semiconductor industry is one of the leading examples who projects modern technology and miniaturization on their products. From enormous size of integrated circuits or ICs to nano size processors that can be found on advanced gadgets we use every single day of our lives. Every individual is committed to achieve satisfaction and quality of their products and services.

On the semiconductor package of LGA's or Land Grid array for micro electromechanical system products, substrate warpage is one of the challenges the manufacturing faces and experience. Substrate warpage as seen on Fig. 1 is the reaction of the material to "bend" or warp after subjecting to oven curing process.

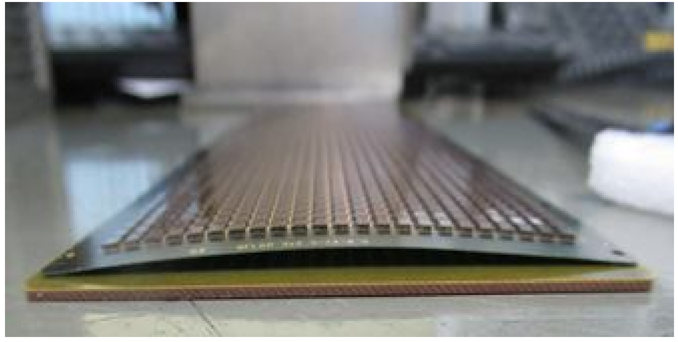


Fig. 1. Warpage visible on substrate after oven curing

High warpage that is already evident after oven curing as shown on Figure 1 is no longer acceptable on the succeeding process step of wire bonding. The warpage measurement acceptance is 1.2mm altitude from the flat surface but the measurement after oven curing is found to be 4.0mm. At time zero, the strip warpage measurement is already at 2.4mm and is already out of acceptance criteria. Based on previous research cited on [1-3] substrate modeling is used to simulate the potential measurement warpage and how it may potentially affect downstream process. It was mentioned also on [4] the improvement of applying heat via oven curing to reduce warpage and have acceptable materials for the next processes. With these research and studies, authors of this manuscript have found an opportunity to study the problem and explore solutions that can be offered related on the substrate revisions.

2. REVIEW OF RELATED LITERATURE

Substrate warpage is one manufacturing issues that were unexpectedly encountered by manufacturing engineers. There are several factors that affect this substrate warpage. Based on the research cited on [5], temperature during oven curing of products is one of factors considered. Several evaluations to use different cuing profile were performed and based on specific material affected, best curing profile was defined. as seen on Fig. 2 from the same citation [5] sample of design of experiments on different temperature profile that contributes to substrate warpage, and its effect.

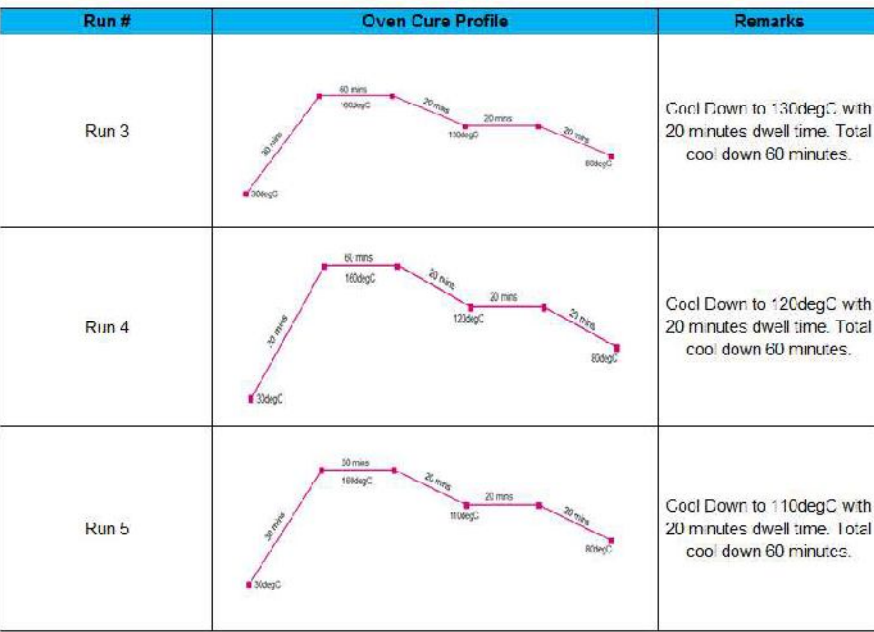


Fig. 2. Design of experiment of different oven curing profile

Other studies performed process improvements by applying weights on the material during heat application. Weights will control the movement of substrate by applying opposing force on the direction of the warpage. This practice as discussed on [6] has been applied and effective on other products but not all results were favorable. That is why the design improvement and modification of core materials is put into play to have robust resolution.

3. METHODOLOGY

Supported by various research and the related literatures as discussed on [7-9], the authors first aim to measure warpage from time zero and see how the measurement behaves as the process progresses at front-of-line (FOL) stations. Shown on Figure 3. is the FOL Process flow generated specifically for this activity where the authors will verify the warpage measurement step-by-step. This includes oven curing of substrate without die and oven curing after die attach.

Fig. 3. Design of experiment of different oven curing profile

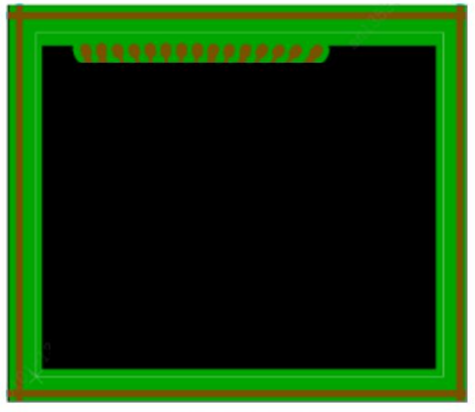
Once strip behavior is comprehended using this process flow, the authors have recommended to validate distinctive designs of solder mask opening (SMO) as consulted and recommended from the supplier. Validation includes the parallel run of the existing SMO design versus the modern designs recommended by the supplier as the SMO design affects the warpage measurement. With this activity, we can compare the performance of both

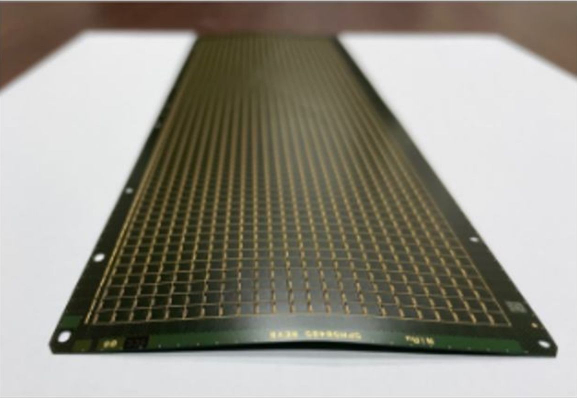
materials and produce a strategic plan to perform the evaluation. Upon result availability, the authors would conclude the best design to demonstrate low warpage measurement given with data results and statistical analysis.

4. RESULTS AND DISCUSSIONS

4.1 Measurement of Strip Warpage for Every FOL Process Steps

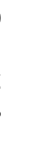
Existing design of substrates has its SMO around each of every unit in the strip. Shown on Figure 4 is the reference substrate design illustration and the warpage condition at Time Zero (T0). At T0, warpage measurement is found with average of 1.6mm.





Solder Mask   Warpage Condition at Time Zero (T0)

Fig. 4. Existing Substrate Design and Warpage Condition



The oven profile of the die attach material used by the product have specific timing and curing temperature known as ramp up, dwell and cool down. These three factors as cited on [10-11] helps the strip to have desirable response of attached die, and substrate condition. Upon process application, the warpage measurement increases when applied with heat along the processes. Curing and cooling helps the strip to be flattened but must meet the target of 1.2mm acceptance warpage altitude of the next process which is wire bonding. This measurement may also result to other problems at wire bond like depressed wire or damaged substrate. As shown on Figure 5. is the behavior of the strip warpage along the process. Three strips were used to validate the warpage results of the existing design of the strip.

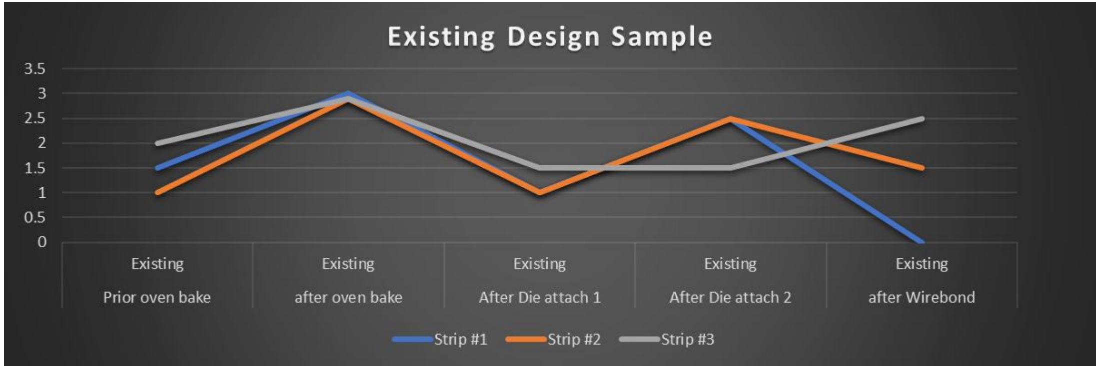


Fig. 5. Existing Design Warpage Measurement per Process Step

With the behavior observed on the existing strip, there will be in need for a drastic improvement from the design level of the core material. the authors have proceeded to assess the recommended innovative designs of substrates aiming to reduce the warpage with respect to the curing time and temperature of the product, and to avoid issues on the next process steps at FOL.

4.2 Identification of the New Designs of Substrates

With the result of the existing substrate design validation performed using several strips, two recommendations were given by the supplier and was considered for evaluation. One modification called as the Scheme 1 pertains to the whole strip where the SMO design is changed on the bottom strip rail, aiming to control the whole warping of the strip. Another modification called as the Scheme 2 pertains to the SMO design changed per unit where gold plated bars were covered by SMO on the long side of the strip. Both designs are shown on Figure 6.

Fig. 6. Improved Substrate Designs for evaluation from substrate supplier

Simulation of both designs at supplier side shows that Option 1 cannot be longer considered as it has no improvement from the existing design. On the other hand, Option 2 proceeded into validation on the assembly line as progress is evident on the simulated results from the supplier. Shown on Figure 7 is the process probability measure for both designs shown that Option 1 is not recommended for further validation and Option 2 can proceed with further analysis.

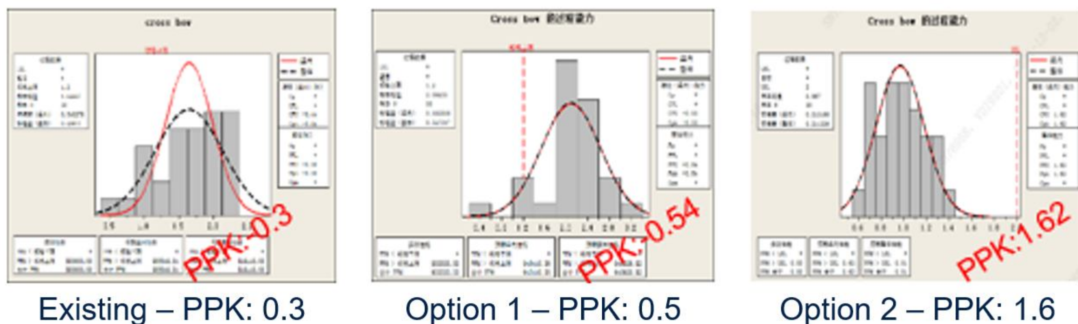


Fig. 7. Process Performance Between Existing and New Substrate Designs

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150 With the data on hand, the authors concurred to continue the validation run of the substrate
151 design of Option 2 which has the higher process capability from the two. Parallel run for
152 existing and considered innovative design will be verified.
153
154 **4.3 Validation Run Between Existing and New Substrate Designs**
155
156 Then new design of substrate from Option 2 is used for validation at FOL. Warpage was
157 measured at every process step as gathered on the existing design. Figure 8. shows that the
158 warpage of the strips has different and improved response where maximum warpage
159 measured is only 1.0mm. Statistical test using One way analysis shown on Figure 9.
160 indicates that there is a significant difference with a P-value of 0.0010 based on the
161 performance between the existing and the new substrate designs with showing that the new
162 substrate design has the lower and favorable results in terms of warpage measurement.
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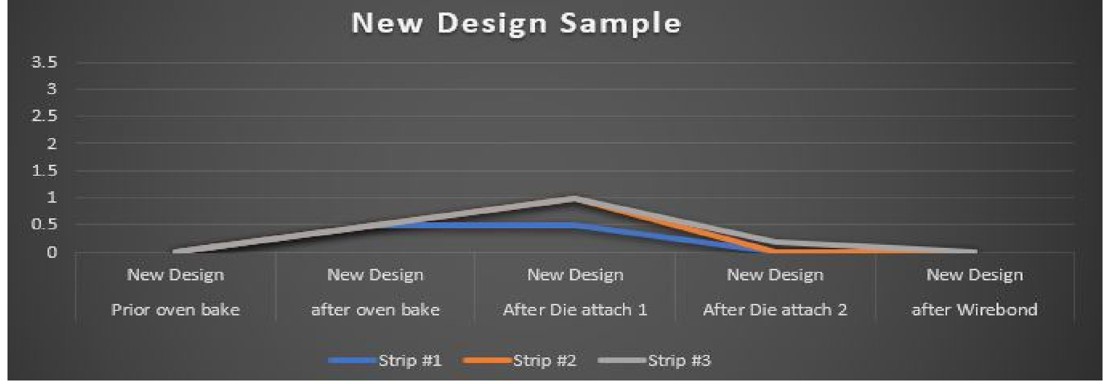

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166 **Fig. 8. New Design Warpage Measurement per Process Step**
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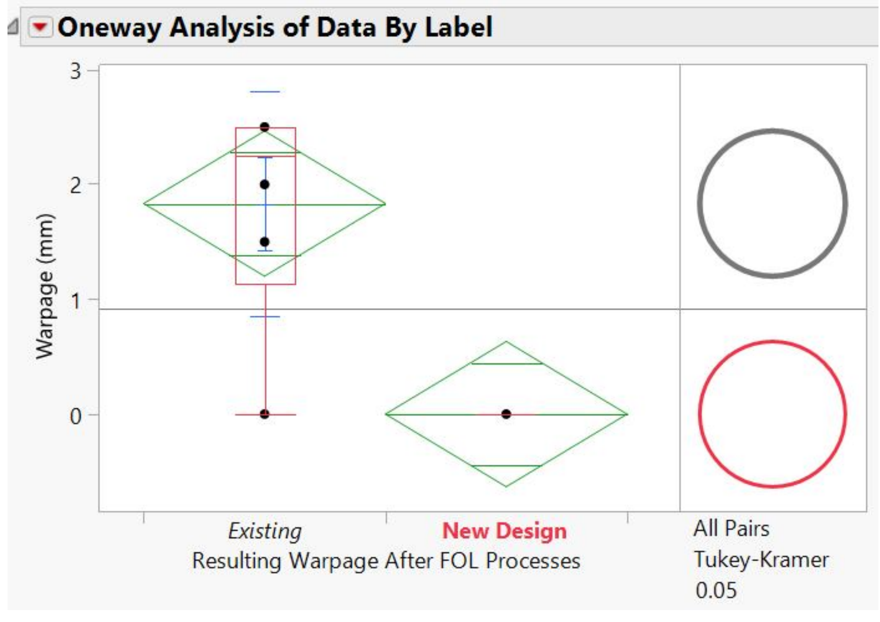

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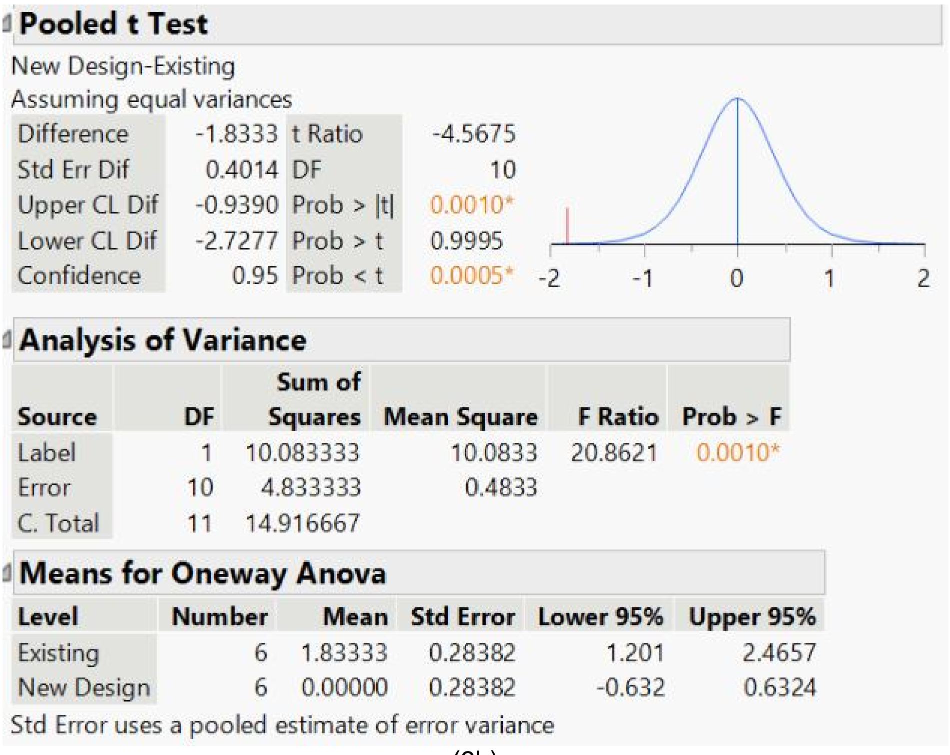
170 (9a)



Pooled t Test

New Design-Existing
Assuming equal variances

Difference	-1.8333	t Ratio	-4.5675
Std Err Dif	0.4014	DF	10
Upper CL Dif	-0.9390	Prob > |t|	0.0010*
Lower CL Dif	-2.7277	Prob > t	0.9995
Confidence	0.95	Prob < t	0.0005*

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio	Prob > F
Label	1	10.083333	10.0833	20.8621	0.0010*
Error	10	4.833333	0.4833		
C. Total	11	14.916667			

Means for Oneway Anova

Level	Number	Mean	Std Error	Lower 95%	Upper 95%
Existing	6	1.83333	0.28382	1.201	2.4657
New Design	6	0.00000	0.28382	-0.632	0.6324

Std Error uses a pooled estimate of error variance

(9b)

Fig. 9(a, b). Statistical Study Results

Additional evidence shown that the study and measurement is valid as warpage was evident on sample photos shown on Figures 10 and 11. Figure 10 is the progress of warpage along the process for existing design from zero to 3.0mm, while Figure 11 shows the progress from new substrate design having a substrate warpage of 1.0mm maximum.

Existing Design of Substrate Results

Fig. 10. Existing Substrate Validation Photos

New Design of Substrate Results

Fig. 11. New Substrate Validation Photos

Data from the evaluation and statistical analysis results show that the substrate design validation described on the methodology is suited for the identification of the acceptable substrate warpage response. With the correct interpretation to choose the best option, it will be a tremendous help to determine the acceptable response for a robust quality product.

5. CONCLUSION AND RECOMMENDATIONS

It has been concluded that the existing substrate design have warpage issues that is related with the SMO. Out of the two new designs recommended by the supplier, it was found out that Option 2 has the most significant result to lower down the warpage but limited and applicable on Front-of-line processes of semiconductor industry. It was noted also that the design of Option 2 with SMO covering the gold-plated bars at the long side of the strip improves the warpage measurement significantly. Studies and research added on the references from other manufacturing is considered significant help to assess and conduct experiments related to die attach oven curing.

In parallel, the authors recommend on consideration of the Option 2 Design of Substrate to lessen the warpage measurement. It is also recommended the validation made on this study to monitor and understand the warpage behavior to verify the design effectiveness.

6. ACKNOWLEDGEMENT

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